COLUMBIA | ENGINEERING
The Fu Foundation School of Engineering and Applied Science

ELEN E3106/4106 Lecture 11

Device Fabrication

Outline

- Finishing up M-S junctions
- Wafer growth
- Photolithography
- Doping processes
- Thin film & metal deposition
- Etching processes

Assignments:

Reading: Streetman and Banerjee §5.1

Homework 4 due tomorrow 10/10 by 5pm

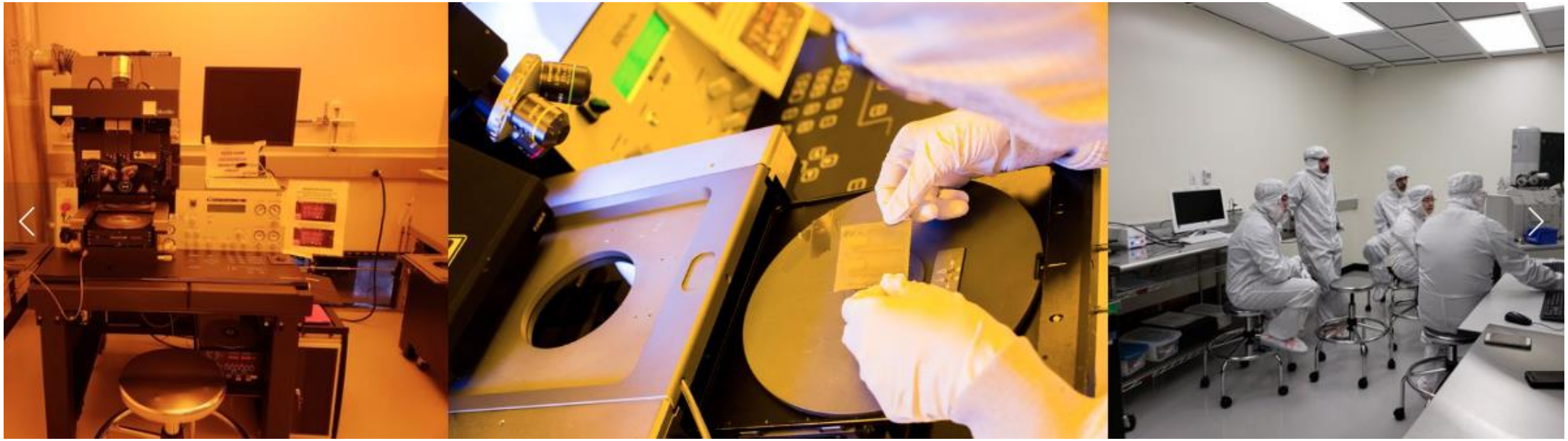
Where does fabrication take place?

- Usually, at a ”fab” facility, inside of a *clean room*
- Clean rooms are required to maintain quality and purity in manufacturing
  - Particle contamination is a major concern when device dimensions are so small
- Typically, you wear a bunny suit
  - Why?

Sources: Wikipedia

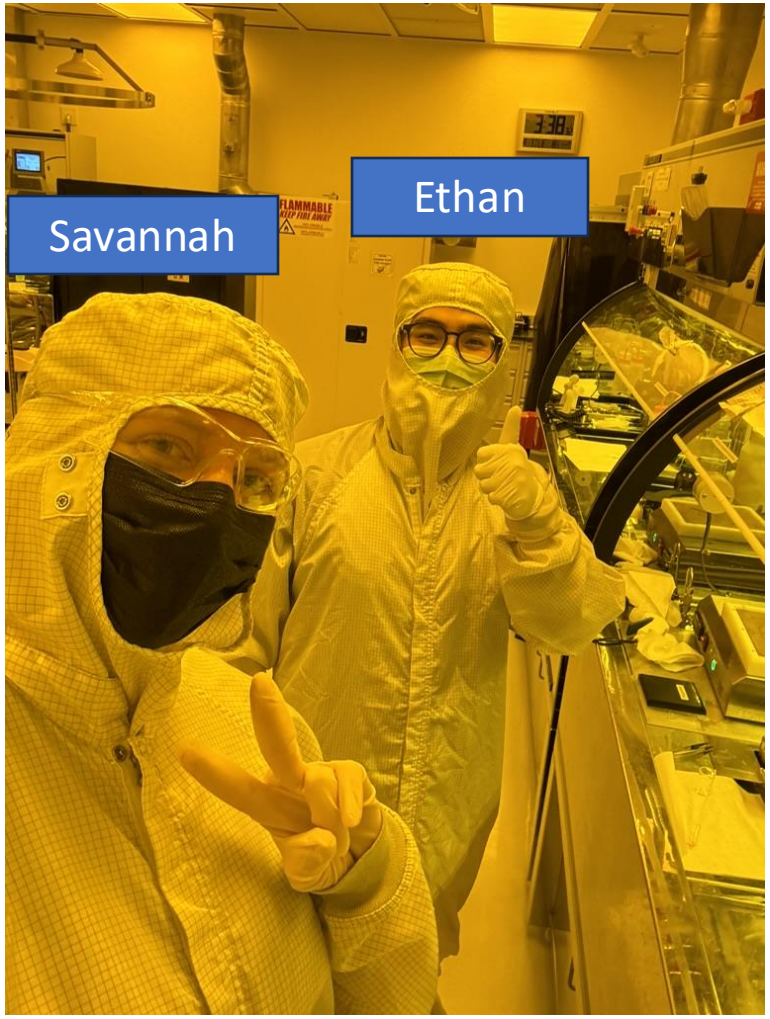
Columbia Nano Initiative Nanofabrication Clean Room Facility

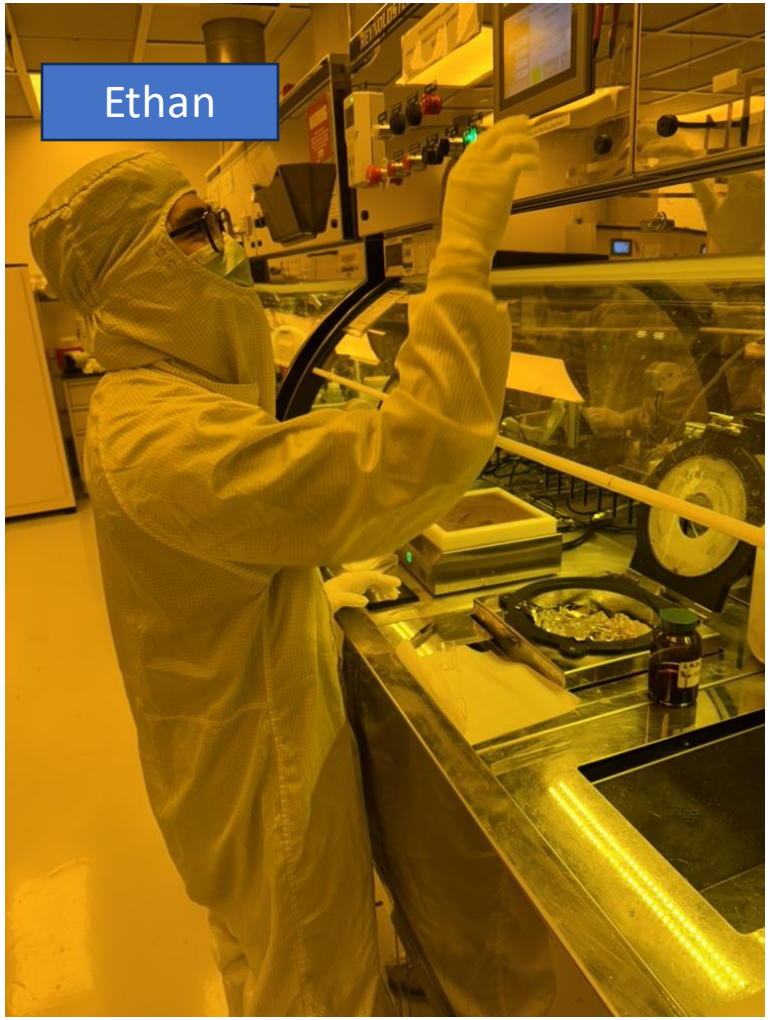
- 5,000-sq. ft. facility in CEPSR
- Built to be class 10,0000 to class 1,000 but measures cleaner
- Supports multidisciplinary research within many academic departments
- Users can also be from industry, government, or other universities



Sources: CNI

3106/4106 Teaching Staff Inside CNI This Week





Test

Contamination Reduction

- Level 1: Clean factories
- Level 2: Wafer Cleaning
- Level 3: Wafer gettering

- International Standard Organization (ISO) specifies cleanroom classifications
- How do we obtain/maintain cleanliness?
  - Air filtration
  - Clean room design
  - Careful elimination of particulate sources

- Typical office building: ISO 8 (Class 100,000)
- State-of-the-art semiconductor facility: ISO 1*

ISO Class Number	≥0.1μm	≥0.2μm	≥0.3μm	≥0.5μm	≥1μm	≥5μm	Equiv FS209 Class
ISO 1	10	2					
ISO 2	100	24	10	4			
ISO 3	10^3	237	102	35	8		1
ISO 4	10^4	2,370	1,020	352	83		10
ISO 5	10^5	23.7×10^4	1.02×10^4	3,520	832	29	100
ISO 6	10^6	2.37×10^5	1.02×10^5	3.52×10^4	8,320	293	1000
ISO 7				3.52×10^5	8.32×10^4	2,930	10,000
ISO 8				3.52×10^6	8.32×10^5	2.93×10^4	100,000
ISO 9				3.52×10^7	8.32×10^6	2.93×10^5	

Table 4.2 ISO (International Standards Organization) cleanroom classification. The number in each cell is the maximum concentration limit (particles/m^3) in the air that are equal to or larger than the specified size. Prior to adoption of the ISO standards, Federal Standard 209 was used for cleanroom specification.

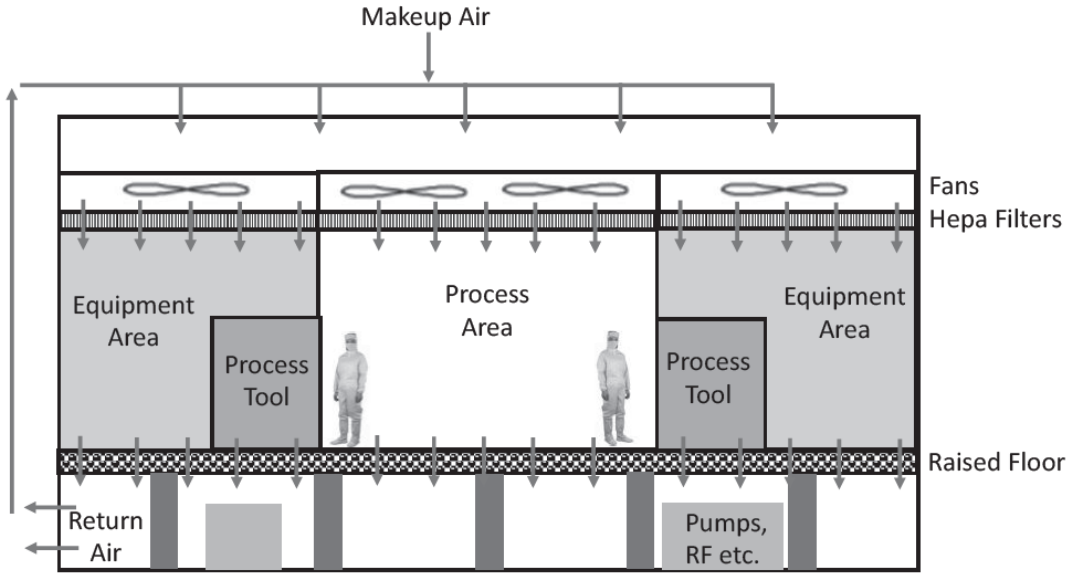
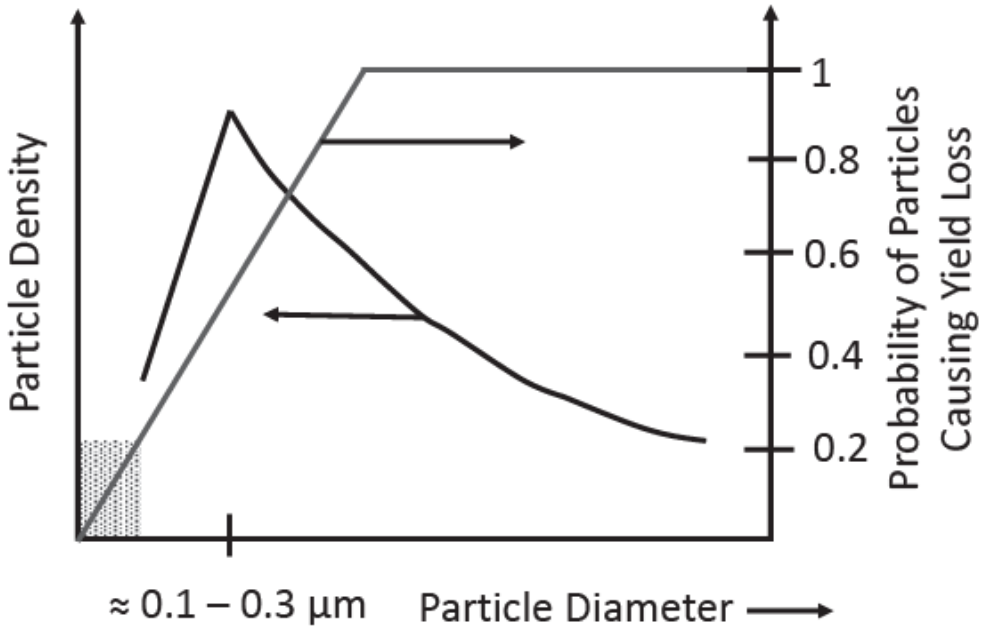


Figure 4.6 Conceptual drawing of a modern semiconductor cleanroom.

Sources: Plummer and Streetman, *Integrated Circuit Fabrication: Science and Technology*

Particle Size Distribution in Room Air

- Particles are always present in a distribution of sizes and shapes
- Estimated that 50-75% of yield loss in is due to particle contamination
- The larger the particle, the higher probability is causes a defect
- Particles between 10 nm and 10 μm are of the most concern
  - Remain suspended for long periods of time
  - Deposit on surfaces through Brownian motion and gravitation sedimentation
- <10 nm: tend to coagulate
- >10 μm: heavy, tend to precipitate quickly

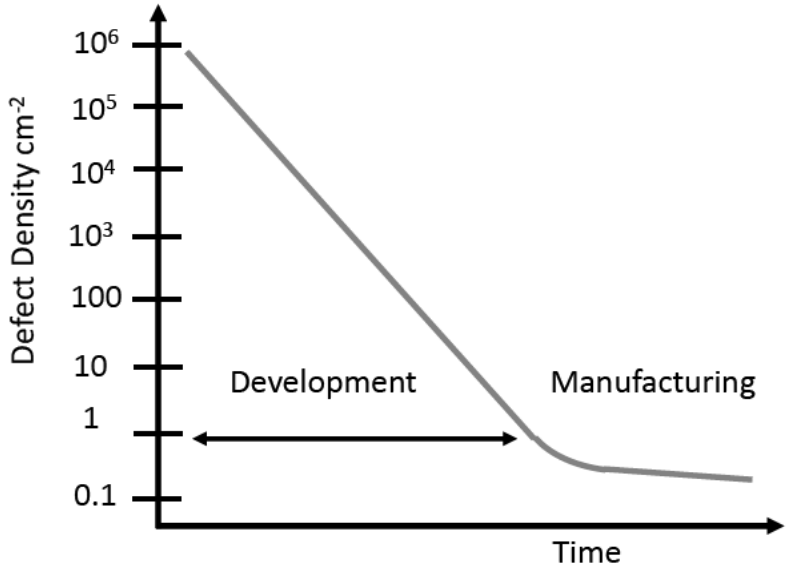


Left axis – Empirical particle size distribution in room air. Right axis – Probability of a particle causing a chip defect.

Sources: Plummer and Streetman, *Integrated Circuit Fabrication: Science and Technology*

Yield

- *Yield* is the fraction of good/usable chips on a wafer
- A single defect can ruin a multi cm^2 size chip
- So, defect densities must be smaller than 1 defect per cm^2!
- Two types of defects: random, and systemic
- Higher yield = more profit
- Desired: Yield > 90%
- Remember: manufacturing is hundreds of steps, and a defect in any one of them could be fatal
  - The yield for any step must be >99%!



Yield improvement occurs during the development phase, where systemic defects are eliminated as the manufacturing process is refined.

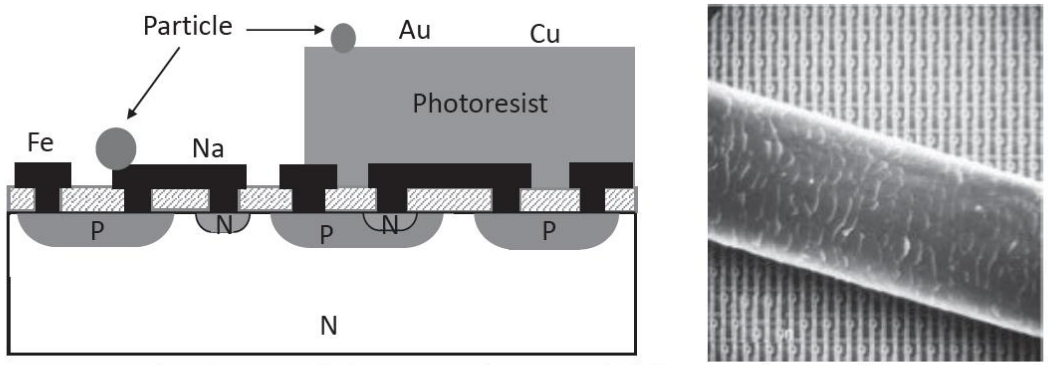


Figure 4.3 Example of some of the contaminants and defect causing particles semiconductor wafers are exposed to during chip manufacturing. The photomicrograph on the right shows a human hair (≈ 50 µm in diameter) on a memory chip. Photo courtesy of © H. Föll (Electronic Materials – Script).

Sources: Plummer and Streetman, *Integrated Circuit Fabrication: Science and Technology*

Modeling Yield and Statistical Process Control

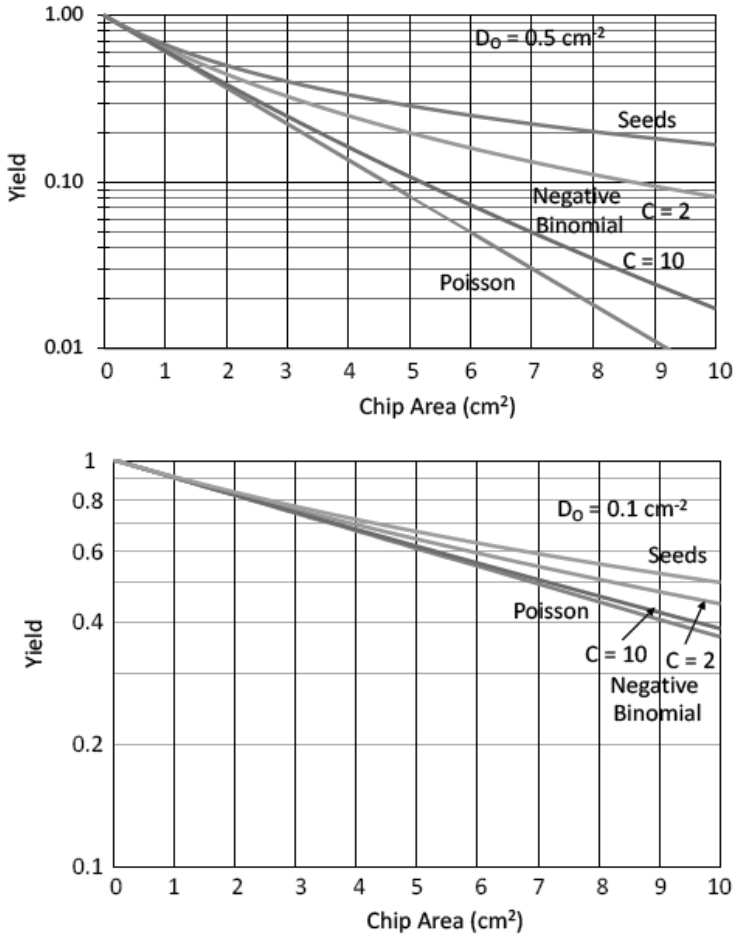


Figure 4.23 Plots of chip yield vs. chip area for various yield models. The defect density is 5X smaller in the bottom plot and the chip yields are correspondingly much higher.

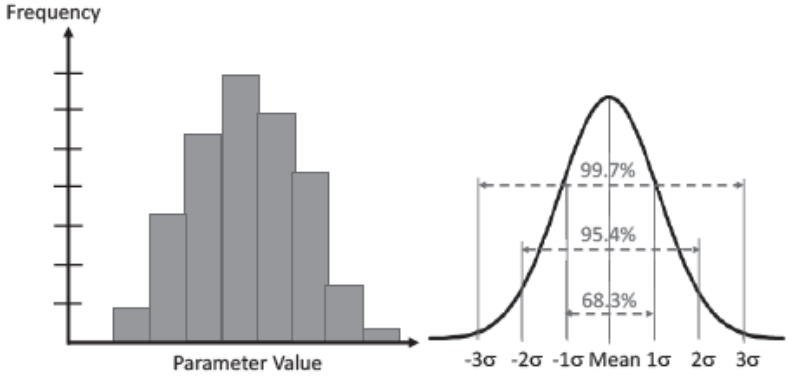


Figure 4.24 Typical distribution of a process parameter such as sheet resistance, oxide thickness, photoresist linewidth etc., resulting from a manufacturing process.

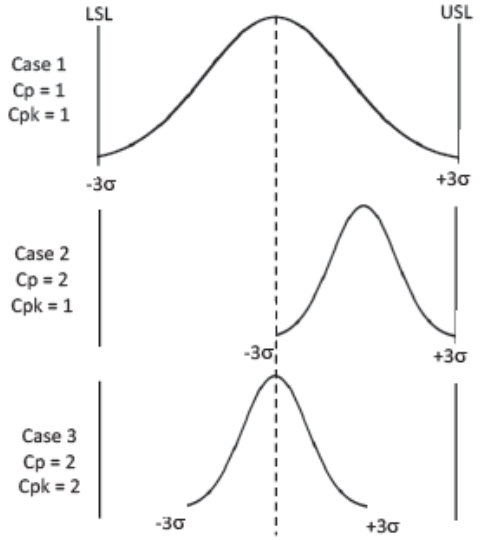


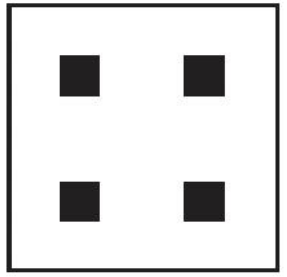
Figure 4.25 Normal parameter distribution examples shown with respect to the upper and lower specification or tolerance limits.

Sources: Plummer and Streetman, *Integrated Circuit Fabrication: Science and Technology*

p-n Diode Fabrication

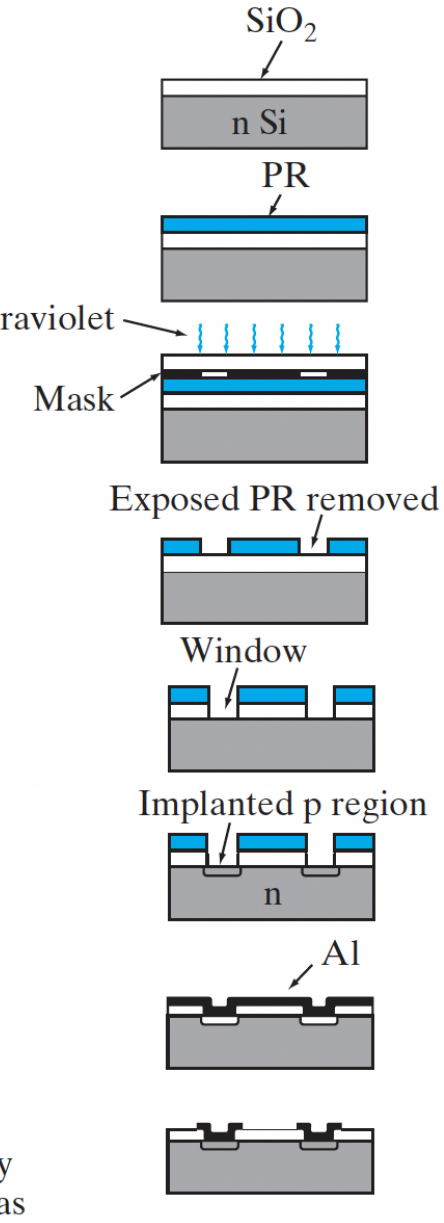
- Only 4 diodes per wafer shown for simplification

Mask A
(doping)



Mask B
(metallization)

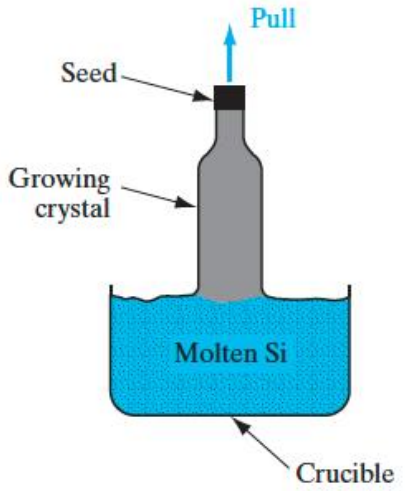
1. Oxidize the Si sample
2. Apply a layer of positive photoresist (PR)
3. Expose PR through mask A
4. Remove exposed PR
5. Use RIE to remove SiO_2 in windows
6. Implant boron through windows in the PR and SiO_2 layers
7. Remove PR and sputter Al onto the surface
8. Using PR and mask B, repeat steps 2–4; etch away Al except in p-contact areas



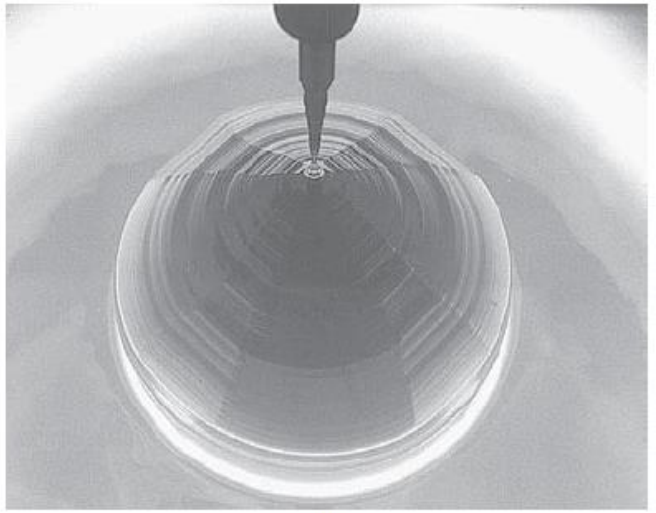
Sources: Textbook

Czochralski Growth Method

- Most common technique for Si and Ge wafer growth
- Reduce raw SiO_2 down to high purity Si
- Heat the Si in a crucible until it melts
- Seed crystal is lowered into the molten material and raised slowly, allow crystal to grow onto the seed
  - Why do we need the seed?
- We end up with a salami-shaped *boule* or single-crystal ingot
  - 12 in diameter, 1 m long, ~300 lbs



(a)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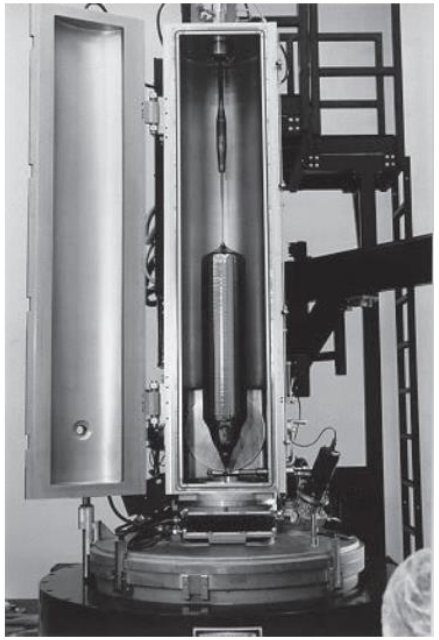


Sources: Textbook, Tokyo Electron

Doping During Growth

- We can add impurities (dopants) into the molten Si
- At the interface between the melt and the solid, there is a distribution of impurities
  - Function of material, impurity, temp, growth rate
- Called the *distribution coefficient*,

$$k_d = \frac{C_S}{C_L}$$

- Impurity concentration in solid:___
- Impurity concentration in liquid:____

Find the weight of As ($k_d = 0.3$) added to 1 kg Si in Czochralski growth for 10^{15} cm^{-3} doping. **EXAMPLE 1–4**

$$\text{atomic weight of As} = 74.9\frac{\text{g}}{\text{mol}}$$

SOLUTION

$$C_s = k_d \cdot C_L = 10^{15}\frac{1}{\text{cm}^3} \rightarrow C_L\frac{10^{15}\frac{1}{\text{cm}^3}}{0.3} = 3.33 \cdot 10^{15}\frac{1}{\text{cm}^3}$$

Assume As may be neglected for overall melt weight and volume

$$\frac{1000\text{g Si}}{2.33\frac{\text{g}}{\text{cm}^3}} = 429.2\ \text{cm}^3\ \text{Si}$$

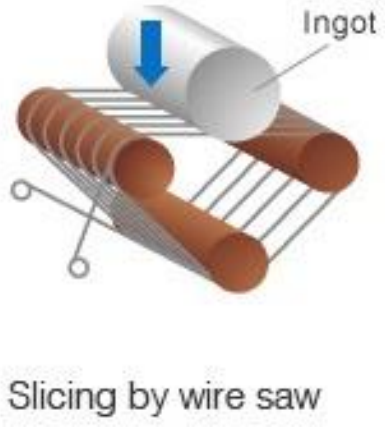
$$3.33 \cdot 10^{15}\frac{1}{\text{cm}^3} \cdot 429.2\ \text{cm}^3 = 1.43 \cdot 10^{18}\ \text{As atoms}$$

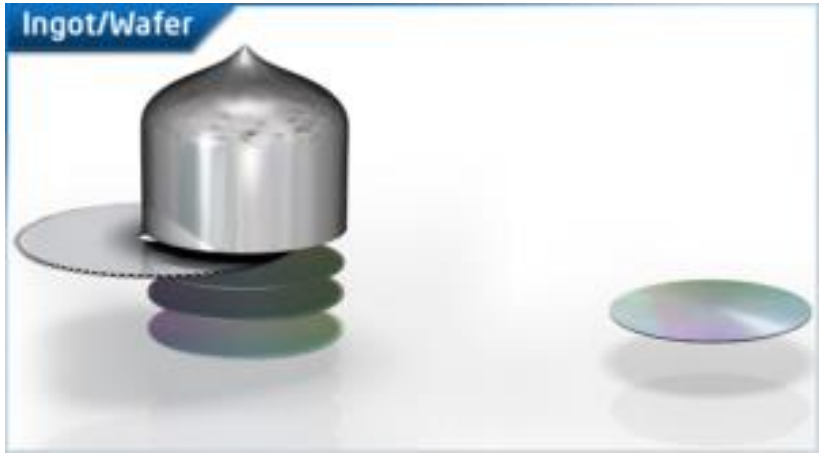
$$\frac{1.43 \cdot 10^{18}\ \text{atoms} \cdot 74.9\frac{\text{g}}{\text{mol}}}{6.02 \cdot 10^{23}\frac{\text{atoms}}{\text{mol}}} = 1.8 \cdot 10^{-4}\text{g As} = 1.8 \cdot 10^{-7}\text{kg As}$$

Sources: C. Hu, *Modern Semiconductor Devices for Integrated Circuits,* Textbook

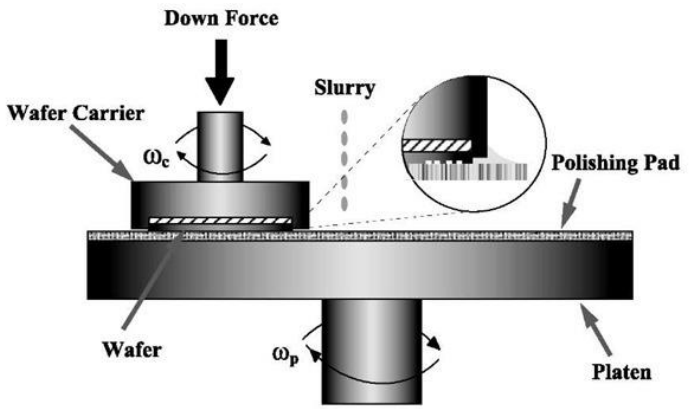
Wafers

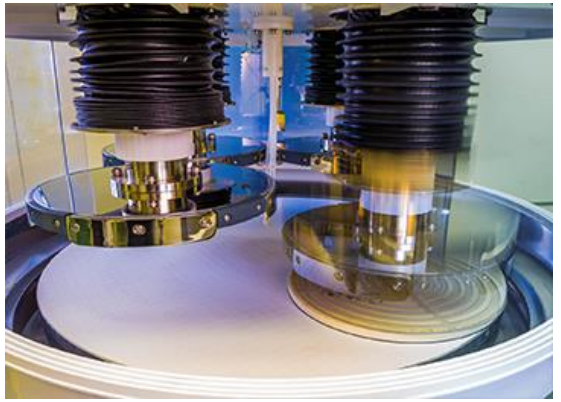
- The notch denoting crystal orientation is ground on on side
- Next, a diamond saw or wire is used to slice the ingot into thin wafers
  - This is why wafers are round!





- Wafers are then lapped and chemically mechanically polished (CMP) on one or both sides to achieve a smooth, mirror-like surface





Sources: Sumco, Silicon Valley Microelectronics, LNF Wiki, Surface Conditioning

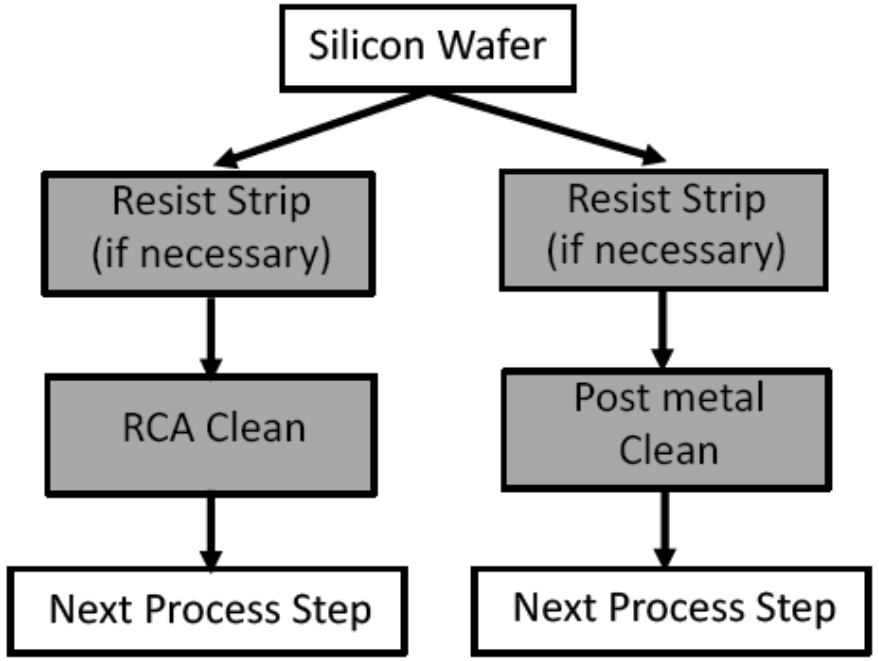
Wafer Cleaning Strategies

- Level 2 of contamination reduction
- After CMP, wafer surface is contaminated by polishing slurry

- Goals of cleaning:
  - Remove particles, like films from photoresist
  - Remove trace contaminations of any other element present on the wafer surface

- More important for front-end processes

- Front-end normally involve high temps (oxidation, anneals, film dep., etc)
- These allow diffusion of contaminants into thin films on the Si or the Si itself!



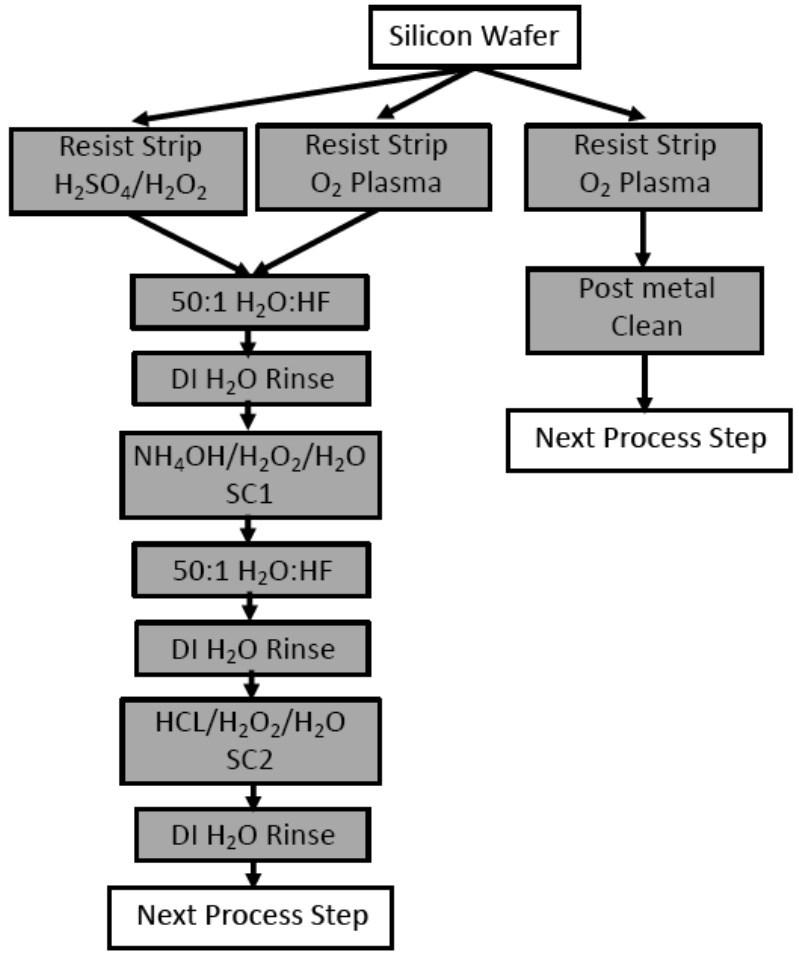
Sources: Plummer and Streetman, *Integrated Circuit Fabrication: Science and Technology*

Wafer Cleaning Strategies

- Photoresist strip
  - PR is an organic polymer
  - Can be moved with an oxygen plasma treatment
  - Or removed by a mixture of hydrogen peroxide (H_2O_2) and sulfuric acid (H_2SO_4)
  - But removal of inorganics like sulfur needs another chemical bath based on hydrofluoric acid (HF)

- RCA Clean
  - Basic cleaning procedure developed by Radio Corporation of America detailed in famous paper in 1970
  - Now the industry standard
  - Uses aqueous-chemical processes involving H_2O_2 mixtures

- Drawback: large chemical consumption!
- Drawback: These chemicals are poisonous and corrosive!



Sources: Plummer and Streetman, *Integrated Circuit Fabrication: Science and Technology*

Thermal Oxidation

- Important step to convert Si to SiO_2
- Takes place in a furnace at high temperatures (~800-1000 °C)
- Oxygenating gas is flowed
- Si is consumed from the surface of the substrate
  - Oxidant molecules diffuse from the top down to the interface
- Important: a stable thermal oxide can be easily grown on Si with excellent interface electrical properties!
- Other semiconductor materials do not have such a useful native oxide

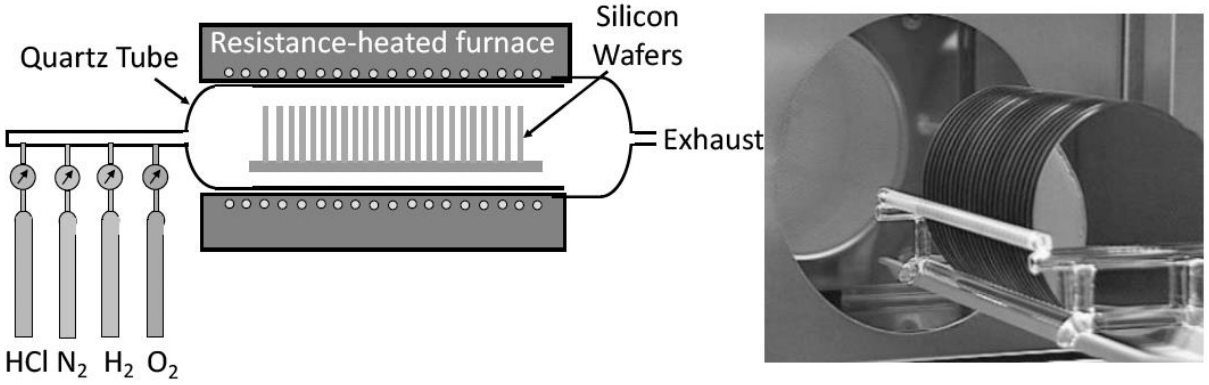
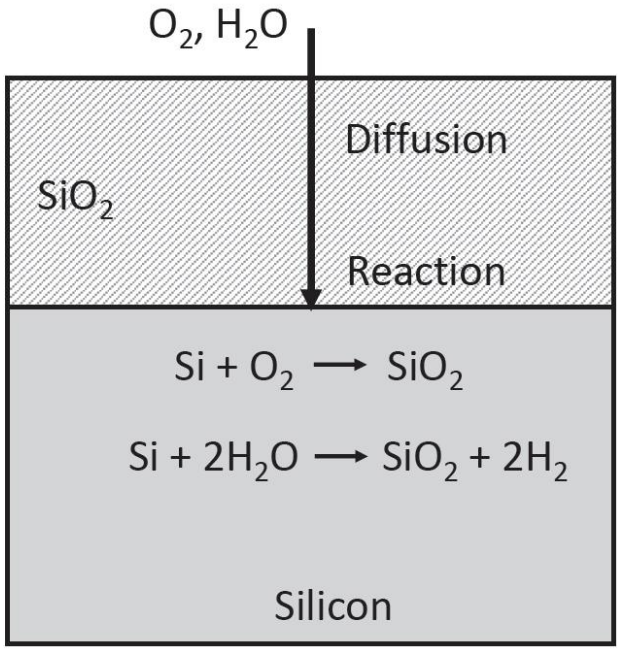


Figure 6.2 Conceptual picture of a thermal oxidation furnace (left). Example of Si wafers being loaded into such a horizontal furnace system (right). Photo courtesy of R. Carranza.



Sources: Plummer and Streetman, *Integrated Circuit Fabrication: Science and Technology*

Doping Strategies

- Method 1: High-temperature diffusion
  - In a furnace, where a gas or vapor source of dopants are introduced
- Method 2: Ion implantation
  - Advantage: can be done at low-T
  - Advantage: can be done selectively (masking)
  - Advantage: for dopants that are hard to diffuse
  - Advantage: precise control of doping concentration
  - *Disadvantage:* lattice damage from ion collisions
    - Can be mitigated by annealing

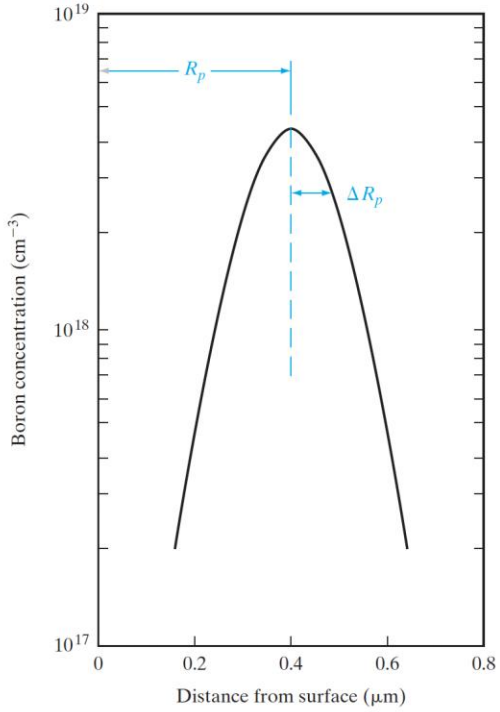


Figure 5–4
Distributions of implanted impurities: gaussian distribution of boron atoms about a projected range R_p (in this example, a dose of 10^{14} B atoms/cm^2 implanted at 140 keV).

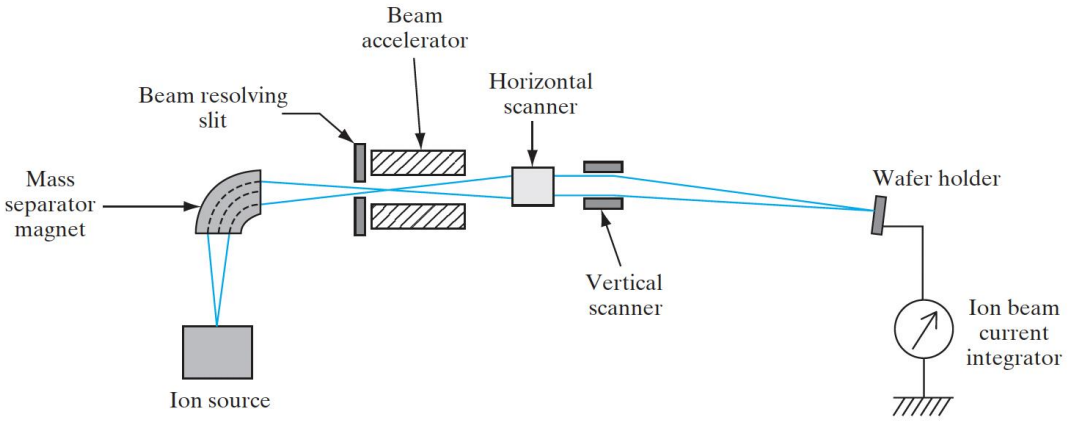
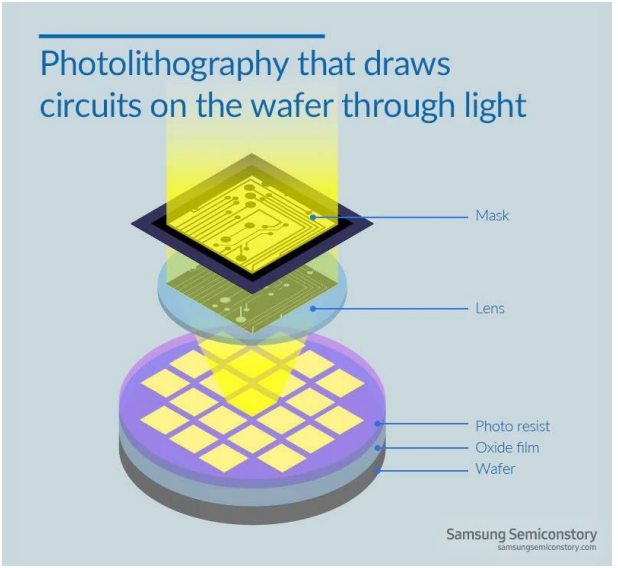


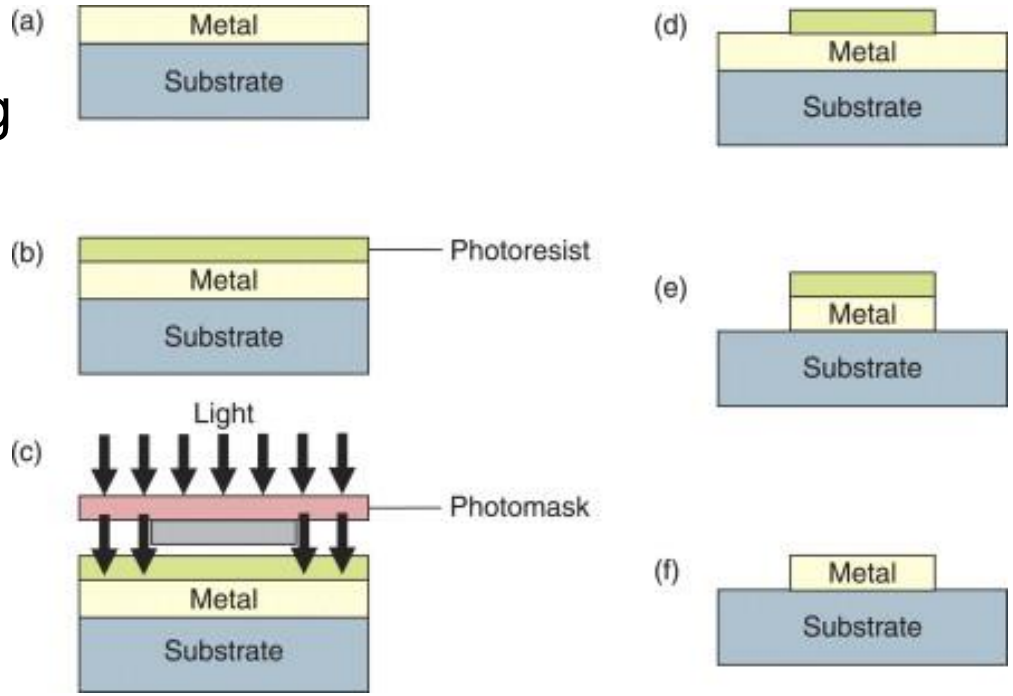
Figure 5–5
Schematic diagram of an ion implantation system.

Sources: Textbook

Photolithography

- Arguably most important step!
- The ability to “print” a nm scale pattern onto a chip with nm scale precision in location
- Process:
  - Light-sensitive photoresist (PR) is spun onto the top of the wafer
  - PR is then selectively exposed by photons passing through a mask that contains pattern information
  - PR is developed in chemicals, which completes pattern transfer from mask onto PR
  - PR can now be used as a mask for the next step (etching, ion implantation, etc.)
- Simple concept, but expensive and difficult to implement!





Sources: Samsung semiconductor, F. Hubenthal, in Comprehensive Nanoscience and Technology, 2011

Photoresists

- Materials designed to change their properties in response to incident photons
- Usually hydrocarbons
- Process:
  - Absorb light
  - Energy from photons break chemical bonds
  - PR chemically restructures into new stable form
- Positive PR = becomes *more* soluble in chemical developer after light exposure
- Negative PR = becomes *less* soluble after exposure
- Multiple ”generations” of resist
  - Diazonaphtoquinones (DNQs)
  - Chemical amplification resists (Cas or CARs)

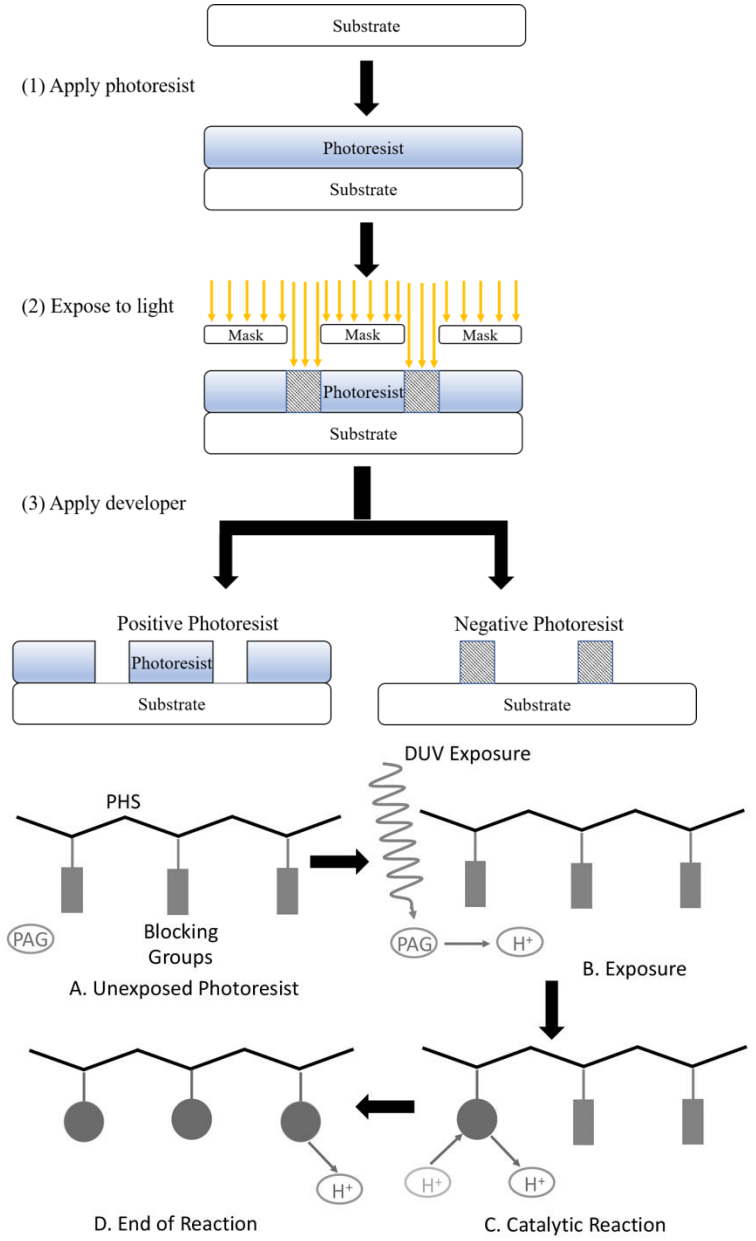


Figure 5.13 Basic operation of a chemically amplified (CA) resist. PAG is the photo-acid generator; the blocking groups are insoluble in the developer. Step c) may repeat tens or hundreds of times during the PEB.

Sources: Wikipedia, Plummer and Streetman, *Integrated Circuit Fabrication: Science and Technology*

Photolithography: Exposure (Illumination)

Demands on…

- Resolution (limits min feature size)
- Exposure field (limits chip size)
- Placement accuracy (each mask must be aligned to features from previous steps)
- Throughput and defect density (impacts yield)

- Issue: diffraction limited geometry
  - When photon wavelength ~ min feature size

- Deep UV (DUV) – 193 nm wavelength
- Extreme UV (EUV) – 13.5 nm wavelength

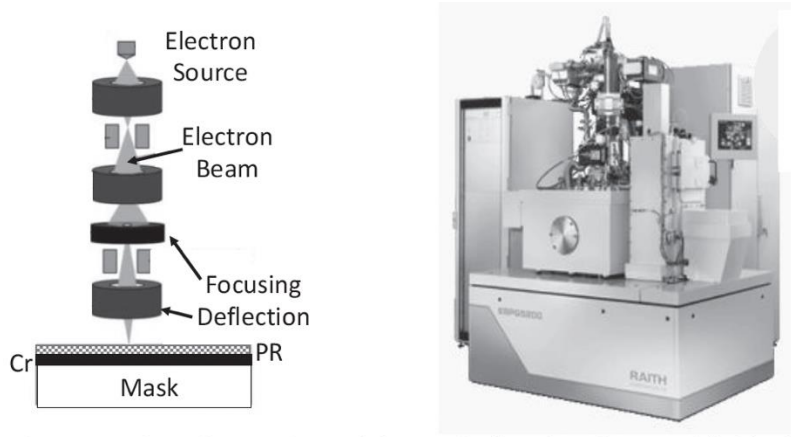


Figure 5.10 Schematic of an electron beam lithography/mask making tool (left). The machine on the right is a Raith product EBPG5200 used for both direct writing on wafers and mask writing. Photo courtesy Raith Corp. Reprinted with permission.

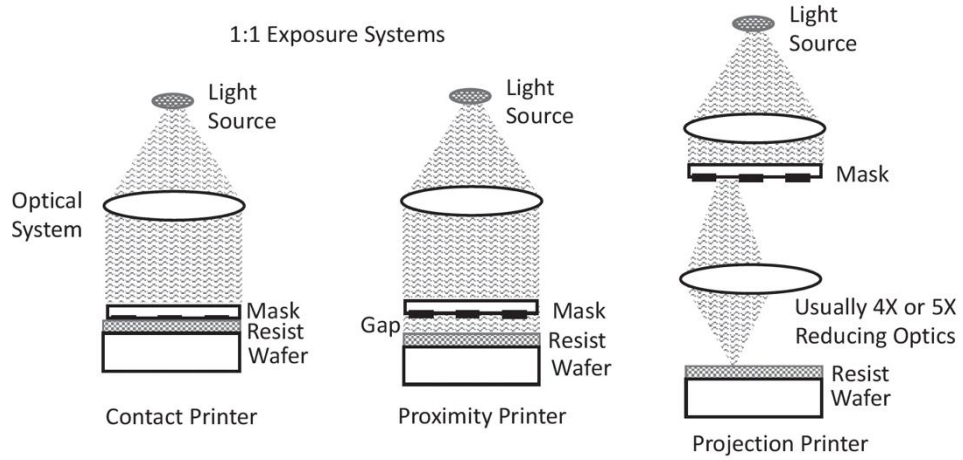
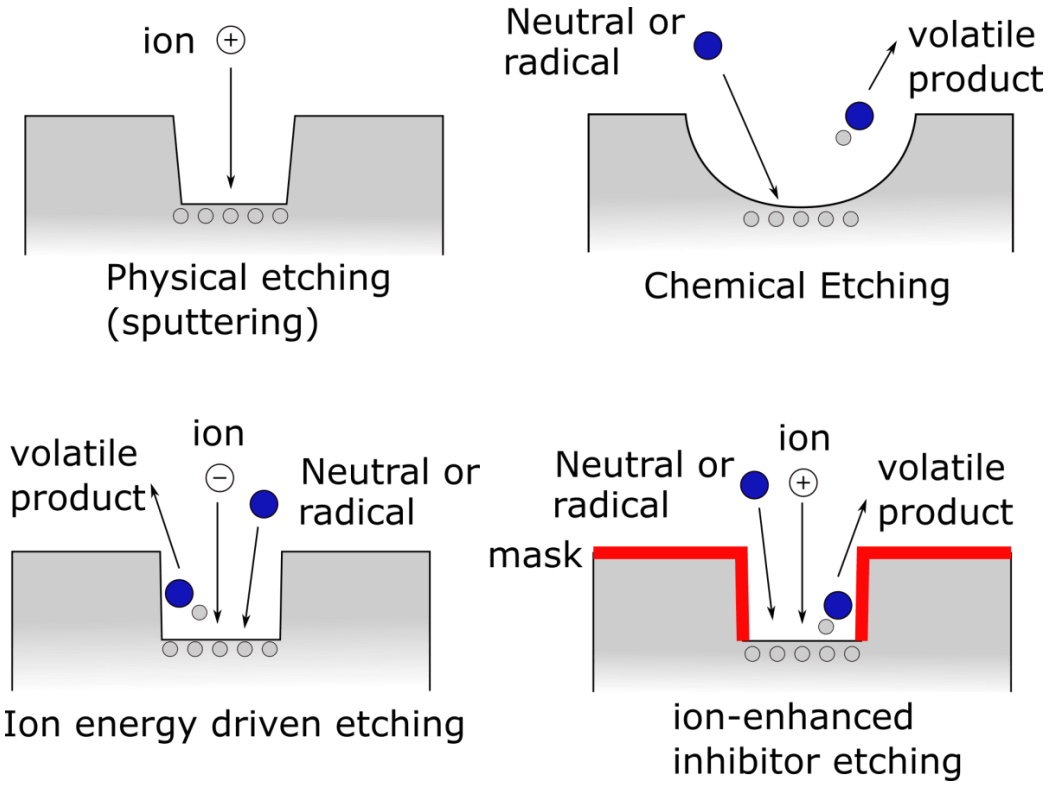


Figure 5.7 Three basic methods of wafer exposure in optical lithography systems.

Sources: Plummer and Streetman, *Integrated Circuit Fabrication: Science and Technology*

Etching Technologies

- *Removing* material
- Wet etching involves chemicals
  - Pro: good selectivity
  - Con: isotropic
- Dry etching (sputtering and plasma-based etching)
  - Pro: anisotropic (higher lateral etch rate than vertical)
  - Con: worse selectivity
- Important parameters: etch rate, selectivity, isotropy
- With plasmas, there are two components to etching:
  1. Physical removal of material through ion bombardment
  2. Chemical reactions between plasma radicals and semiconductor remove material
  - *Reactive ion etching* (RIE) combines both



Sources: PV Education

Thin Film Deposition Techniques

- *Depositing* material
  - Dielectrics, passivation layer, etc.
- What's the difference from thermal oxidation?
  - Doesn't consume the Si itself
  - Can be done at lower temps
  - Sometimes Si is already inaccessible at later steps
- Common techniques:
  - Chemical vapor deposition (CVD)
  - Atomic layer deposition (ALD)
- Usually polycrystalline or amorphous films
  - Except special cases, like metal-organic CVD (MOCVD)

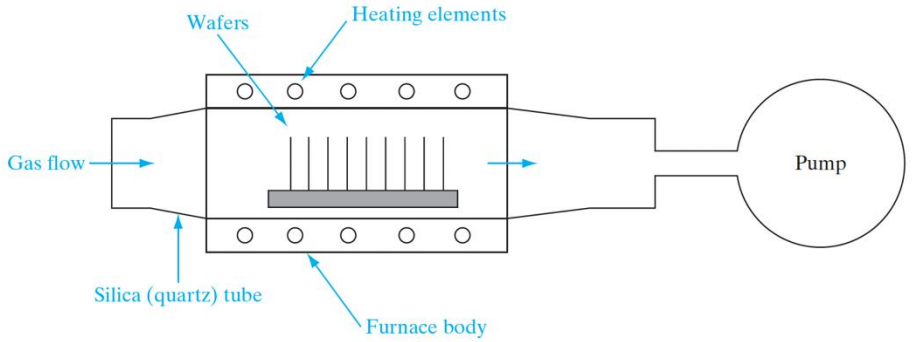
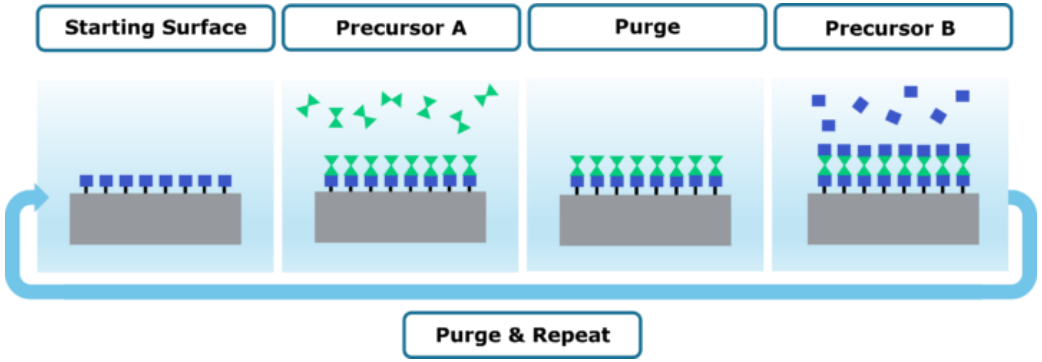


Figure 5–6
Low-pressure chemical vapor deposition (LPCVD) reactor.



Sources: Textbook, Beneq

Metallization

- *Depositing* metals, usually to form the contacts
- Remember, we have to be able to connect to devices (and connect them to each other in an IC)
- M-S junctions created by physical deposition of metals through
  - Sputtering
  - Electron beam evaporation
  - Electroplating

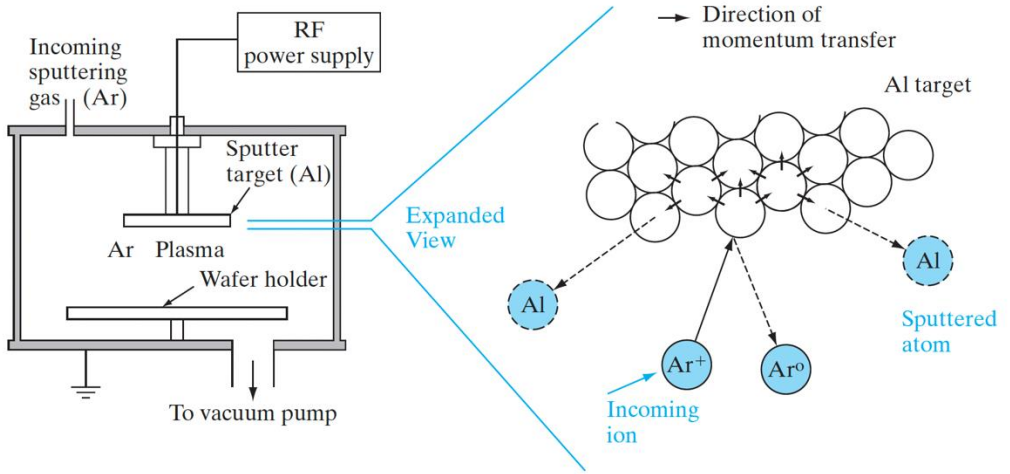


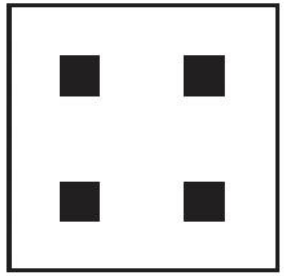
Figure 5–9
Aluminum sputtering by Ar^+ ions. The Ar^+ ions with energies of ~1–3 keV physically dislodge Al atoms which end up depositing on the Si wafers held in close proximity. The chamber pressures are kept low such that the mean free path of the ejected Al atoms is long compared to the target-to-wafer separation.

Sources: Textbook

p-n Diode Fabrication

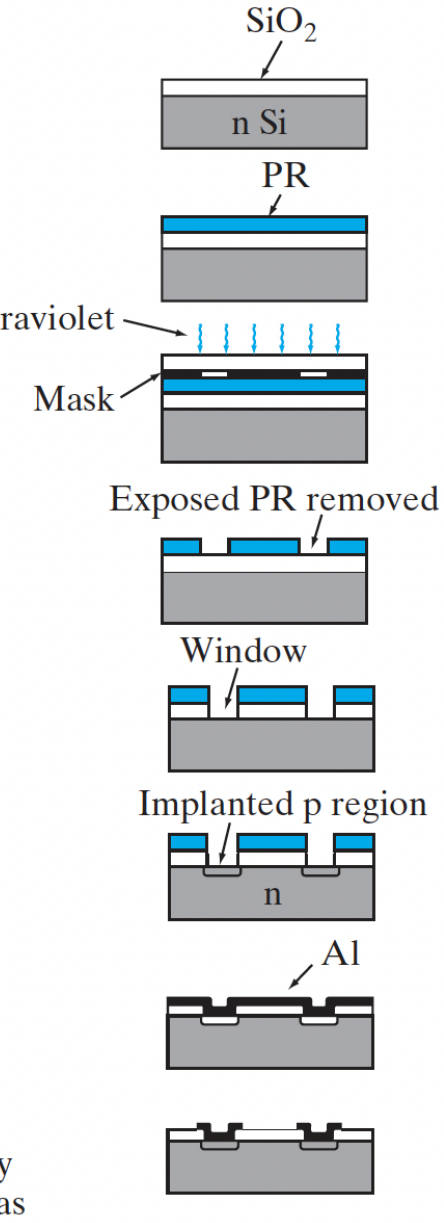
- Coming back to this slide again…
- Only 4 diodes per wafer shown for simplification

Mask A
(doping)



Mask B
(metallization)

1. Oxidize the Si sample
2. Apply a layer of positive photoresist (PR)
3. Expose PR through mask A
4. Remove exposed PR
5. Use RIE to remove SiO_2 in windows
6. Implant boron through windows in the PR and SiO_2 layers
7. Remove PR and sputter Al onto the surface
8. Using PR and mask B, repeat steps 2–4; etch away Al except in p-contact areas



Sources: Textbook

More info on device fabrication technology

- Textbook: *Integrated Circuit Fabrication: Science and Technology* by Plummer and Griffin
  - Limited version for free download: https://plummergriffinbook.stanford.edu/
- Grad students: ELEN E4944: Principles of Device Microfabrication